



## Hardware Design of the PMSM Control System Based on DSP and CPLD

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**Abstract:** This paper designs and realizes the hardware of a PMSM control system, in which DSP is the main controller and CPLD is the auxiliary logic controller. The proposed power driver consists of three independent H-bridge inverter drive circuits. The hardware are designed including the motor phase current detection, main voltage monitoring, signal acquisition of both rotor position and speed, overcurrent protection and other related circuits. The experimental results show that the motor controller is reliable and stable with strong practicability.

**Keywords:** Control System; CPLD; DSP; PMSM

### I. INTRODUCTION

Along with the progress of the society and the development of science and technology, the motor has been widely used in various industries, such as industrial, agriculture, transportation, and other major industries in national economy. Into the 1980's, with the rapid development of permanent magnetic material and the decrease of cost, especially iron shed material, which has excellent performance and low price, these advantages greatly promote the development of permanent magnet synchronous motor and fully meet the modern high performance servo system of high precision control requirements of motor speed and requirements of Control system with high reliability [1]. Therefore, the permanent magnet synchronous motor with its excellent performance, combined with modern drive control technology and high precision sensor technology, forms the most excellent servo control system and it has become the mainstream and development direction of modern high performance servo control system [2-6]. In this paper, the permanent magnet synchronous motor control system with high reliability is designed, and it has a certain fault tolerance function. The system uses DSP as the core control device, supplemented by CPLD logic control. Periphery circuit consists of current detection, voltage monitoring, speed and position detection circuit, and power drive circuit, etc.

### II. SYSTEM STRUCTURE

The block diagram of permanent magnet synchronous motor control system is shown in Fig. 1.

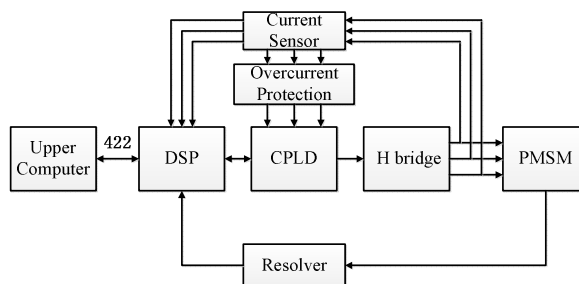


Fig. 1 The block diagram of PMSM control system

Upper computer and DSP exchange data through RS-422 bus. The upper computer sends the speed control command to the DSP, and DSP send the motor speed, the current position of the rotor, the motor current of each phase and the main voltage to the upper computer. These data will be displayed in the window of the upper computer. DSP converts the speed control instructions to the corresponding PWM signal. After the treatment of CPLD, the PWM signal control the switching of IGBT through the driver chip, and then control the motor. This system uses the speed, current double closed-loop control. For the current closed-loop control, the current sensors are used to detect the three-

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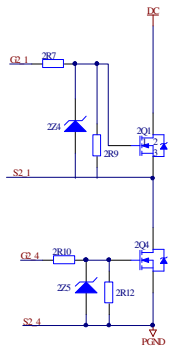


Fig. 3 Half bridge circuit

**C. Current Detection Circuit**

In order to realize the current closed-loop control and overcurrent protection, the circuits for detecting phase current is required. The current sensor uses Allegro's ACS723-20AB. It is a high accuracy, galvanically isolated current sensor IC. Its measuring range is from -20A to 20A. When the current is 0A, the output voltage of the sensor is  $V_{cc} \times 0.5$ , where  $V_{cc}$  is the power supply voltage of the sensor. The sensitivity of the sensor is 100mV/A. Therefore, when the current is I (A), the output of the current sensor VI is as follows:

$$VI = V_{cc} \times 0.5 + I \times 0.1$$

The power supply voltage of current sensor is 5V, while the maximum voltage that DSP's ADC port can withstand is 3.3V. Therefore, the output voltage range of current sensor should be converted to the range of the ADC port level. By using rail to rail operational amplifier OPA340 and flexible configuration of the resistance, the range of VI can be scaled to 3.3V. The current detection circuit is shown in Fig. 4. IP+ and IP- are connected in series with the motor winding circuit. The sensor has the pin-selectable band width: 80 kHz for high bandwidth applications or 20 kHz for low noise performance. The BW\_SEL pin can be used to select one of the two bandwidths to optimize the noise performance.

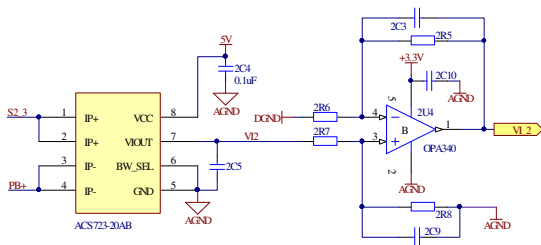


Fig. 4 Current detection circuit

**D. Overcurrent Protection Circuit**

The supply voltage of the system is 280V. Therefore, the protection circuit is very important. The overcurrent will cause great damage to the whole system and the damage is often unrecoverable. In order to avoid such damage, the overcurrent protection circuit needs to be designed. The overcurrent protection circuit of the system consists of a Schmidt trigger and the internal logic of CPLD. The schematic diagram of overcurrent protection circuit is shown in Fig. 5.

This circuit uses AD8468, which is one rail-to-rail, fast, low power, single-supply TTL/CMOS comparator. The Schmidt trigger consists of two comparators.  $V_{ref1}$  and  $V_{ref2}$  represent respectively the maximum current peak and the minimum current peak under normal conditions.  $VI_2$ , the output value of the current sensor that has been converted, compares with the two thresholds and then gets two error signals, FAULT1\_1 and FAULT1\_2. These two signals go directly to CPLD. Under normal conditions, FAULT1\_1 should be high and FAULT1\_2 should be low. At this time, the PWM signal corresponding to this phase current output normally. When  $VI_2$  exceeds one of the two thresholds, PWM signal corresponding to this phase current will be banned in CPLD to prevent damage to the device.

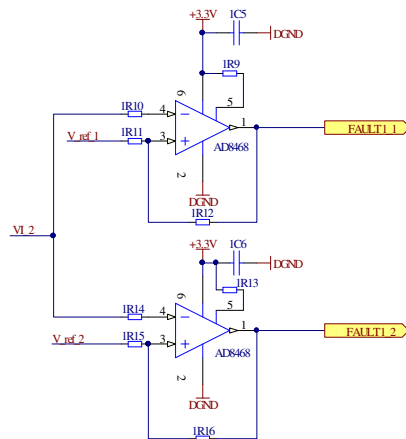


Fig. 5 Overcurrent protection circuit

**E. The Voltage Detection Circuit of the Main Circuit**

The voltage detection circuit of the main circuit uses the way of resistance divider detection. Voltage signal generated by resistance voltage divider is used as the input of the isolation operational amplifier. The output

of the isolation amplifier is a pair of differential signals, SYS\_V\_P and SYS\_V\_N. They go directly to the ADC port of DSP. The circuit is shown in Fig. 6. The isolation operational amplifier uses TI's AMC1200. It is a precision isolation amplifier with a fixed gain of 8, differential input and differential output. The input range of this isolation amplifier is  $\pm 250\text{mV}$ . Therefore, we should pay attention to the selection of the resistance value of the divider resistance. The role of the zener 5Z1 is to prevent the input from exceeding the limit and ensure that the equipment is not damaged. The role of the capacitor 5C2 is to filter out the ripple noise on the voltage signal [8].

The mathematical relationship between the input voltages and the output voltages is:

$$V_{OUTP}-V_{OUTN}=8 \times (V_{INP}-V_{INN})$$

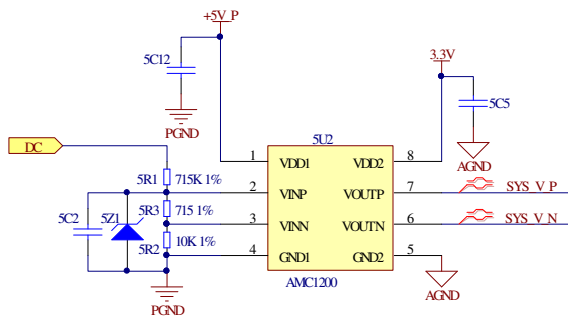


Fig. 6 The voltage detection circuit of the main circuit

#### F. Velocity and Position Detection Circuit

It can't meet the needs of the system as only using current closed-loop control, therefore, the control strategy of the speed and current double closed loop is often used. In order to realize the speed closed-loop control, the velocity information is required to be detected in real time. The velocity and angle information can be obtained in real time by using a rotary transformer [9].

The AD2S1210 is a complete 10-bit to 16-bit resolution tracking resolver-to-digital converter, integrating an on-board programmable sinusoidal oscillator that provides sine wave excitation for resolvers. The converter accepts  $3.15\text{Vp-p} \pm 27\%$  input signals, in the range of 2kHz to 20kHz on the sine and cosine inputs. A Type II servo loop is employed to track the inputs and convert the input sine and cosine information into a digital representation of the input angle and velocity. The maximum tracking rate is

3125rps. This chip is compatible with the SPI standard of DSP, so DSP can read the current speed and angle of the motor by SPI in real-time. AD2S1210 outputs the differential excitation signal. Due to the limitation of the chip's drive ability, the current drive ability must be enhanced by the external buffer circuit. The low distortion, high output current, and wide output dynamic range make the AD8397 ideal for applications that require a large signal swing into a heavy load. The buffer circuit is shown in Fig. 8.

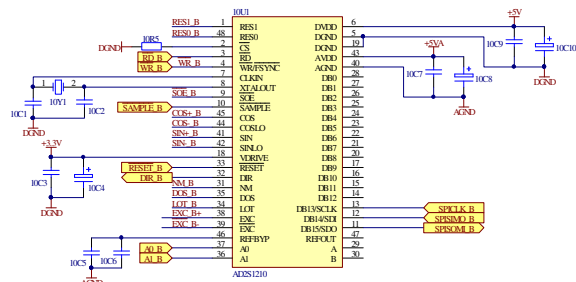


Fig. 7 Resolver-to-digital converter AD2S1210

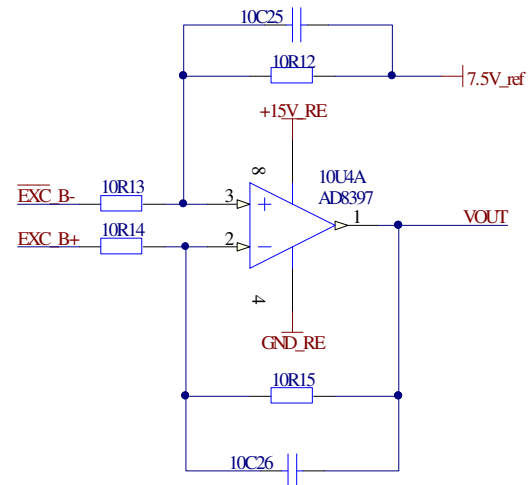


Fig. 8 One way buffer circuit of differential excitation signal

#### IV. EXPERIMENT RESULTS AND ANALYSIS

The experiment takes a three-phase six pole permanent magnet synchronous motor as the control object, using the speed and current double closed-loop control. Fig 9 shows the waveform of the over current protection signal. In Fig 9, channel 1 is the original output VI of the current sensor, which ranges from 0V

to 5V; channel 3 is the converted output V\_I of the current sensor, which ranges from 0V to 3.3V; channel 2 is a signal called FAULT, which corresponds to the threshold VT+. Normally, The FAULT signal is a high level signal. The line labeled b represents VT+. When V\_I is higher than VT+, the Schmidt trigger is triggered, meanwhile, the FAULT signal changes from a high level to a low level, and then the PWM signal of this phase will be banned in the CPLD.

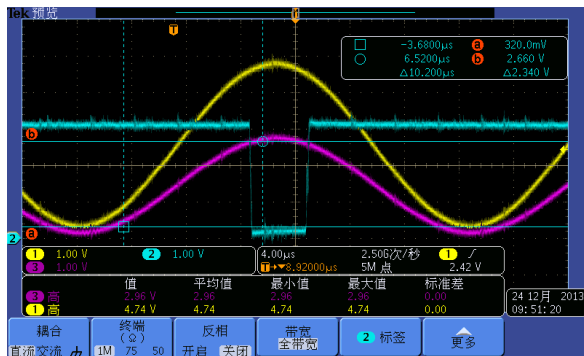


Fig. 9 Overcurrent protection signal

Fig 10 shows the gate drive signal of the H-bridge. Channel 2 is the gate drive signal of one low side IGBT of the phase A. Channel 3 is the gate drive signal of one low side IGBT of the phase B. Channel 4 is the gate drive signal of another low side IGBT of the phase B. Channel 3 and channel 4 is basically complementary and the tiny gap between the edge is the dead time.

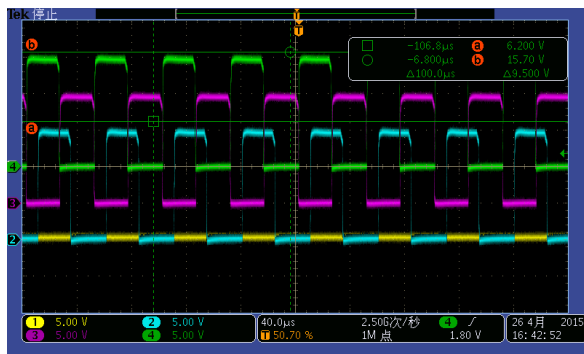


Fig. 10 The gate drive signal of the H bridge

Figure 11 shows the waveform of each phase current when the motor speed is 9400r/min. Channel 1 is the position signal that converted from the real-time angle value. This signal is high from 0 degrees to 180

degrees, and it is low from 180 degrees to 360 degrees. Channel 2 is the current waveform of the phase A. Channel 3 is the current waveform of the phase C. Channel 4 is the current waveform of the phase B. From these waveforms we can see that, these phase currents are in accordance with current sinusoidal trend and all phases tally with the actual situation. If the control program is further optimized, the control effect can be better.

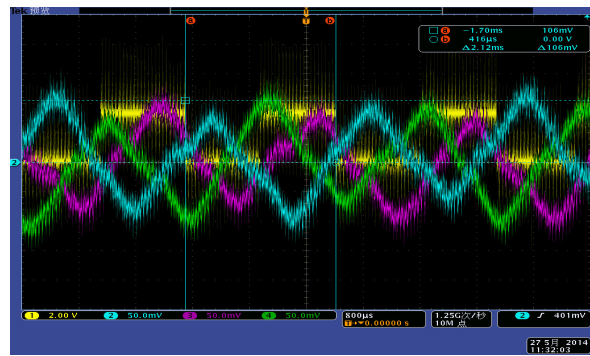


Fig. 11 The waveform of each phase current when the motor speed is 9400r/min

## V. CONCLUSIONS

The hardware of a PMSM control system is designed and realized, where DSP is applied as the main controller and CPLD as the auxiliary logic controller. On the view of the actual operating effect, the system can realize the high precision speed control of the permanent magnet synchronous motor. And it is of good stability, high reliability and strong practicability.

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